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# A single-bit sampling demodulator for biomedical implants

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ABSTRACT

A phase-shift keying (PSK) demodulator is demonstrated for the target application of low power and high data rate inductive links. The demodulator based on the single-bit sampling demodulation scheme is capable of operating in binary, quadrature, 8-, and 16-PSK mode. The prototype chip realized in 0.18-μm CMOS process can demodulate up to 1.25 MSymbol/s at 5-MHz carrier frequency. It occupies $240 \times 310\ \mu m^2$ and consumes 140 μA from 1.2 V.

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## 1. Introduction

There are great interests for biomedical devices that can be implanted inside the human body such as retinal implant, cochlear implant, sphincter sensor, glaucoma sensor, intracranial pressure sensor system, functional electrical stimulation systems, and activity monitor and laboratory system [1]. Many of these devices need links to the external world for power delivery as well as data communication. For example, a retinal prosthesis continuously transmits video streaming data and a large amount of power in order to stimulate optic nerves using many electrodes [2,3]. In such an application, wireless power transmission is an attractive solution.

In order to avoid any damage to human body by power delivering, 1–10 MHz is often used since this frequency range has the least amount of absorption in skin [4]. Inductive links are widely used in this band. While power and data can be transferred through separate links for efficient power transmission [3,4,7,11,12], a single link transferring data and power simultaneously offers a simpler structure [2,5,8,10], which is of great advantage for implantation applications. Fig. 1 shows a block diagram for an inductive link composed of two magnetically coupled coils across skin. Both external and implanted units have data modulation and recovery blocks while only the implanted unit includes power recovery block. To transmit data and power simultaneously downlink (from the external unit to the implanted device), constant-amplitude modulation schemes such as pulse-width modulation [2], frequency-shift keying (FSK) [5–7] and phase-shift keying (PSK) [8–11] are often used since they are compatible with rectifier-based power recovery [8].

In most inductive-link transmitters and receivers reported so far, low-order modulation schemes such as amplitude-shift keying, FSK, binary phase-shift keying (BPSK) and quadrature phase-shift keying (QPSK) have been used. However, in applications where power and data are transmitted through the same coil, the available bandwidth is limited due to the power transfer efficiency consideration. Consequently, high-order modulation schemes that can enhance the total data rate without requiring more bandwidth is highly desirable. However, the conventional high-order demodulation techniques that are commonly used in communication systems cannot be adapted for implantation applications since they require a significant amount of power consumption.

We have previously demonstrated single-bit-sampling-based BPSK and QPSK demodulator for high-speed data communication applications [13–15]. In this paper, we extend our demodulation scheme so that it can be used for bio implantation applications with high spectral efficiency and lower power consumption. Our prototype demodulator, fabricated in TSMC 0.18-μm CMOS, can successfully demodulate 1.25-Mb/s binary, quadrature, 8-, and 16-PSK data using 5-MHz carrier frequency.

This paper is organized as follows. Section 2 explains our demodulation scheme based on the constellation diagram, and Section 3 describes implementation of the prototype chip. Section 4 gives measurement results and conclusion is given in Section 5.

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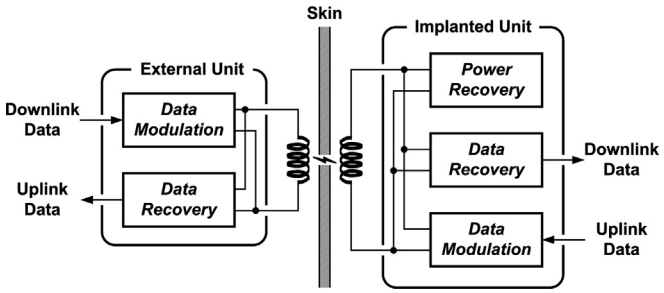
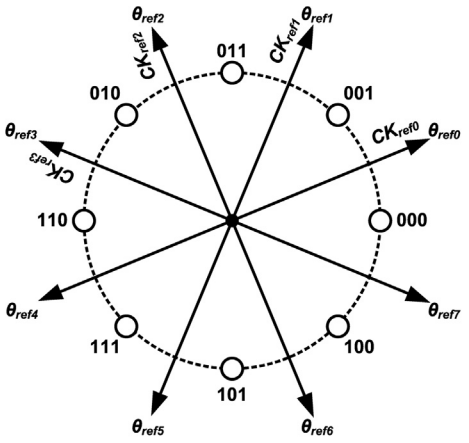



**Fig. 1.** Inductive link.

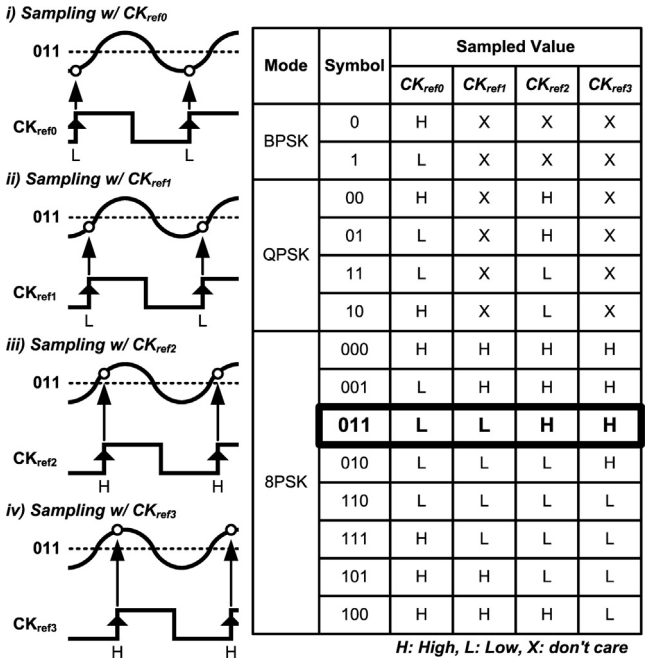



| Symbol | Sign of ($\theta_{input}$ - $\theta_{ref\,n}$) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $\theta_{ref0}$ | $\theta_{ref1}$ | $\theta_{ref2}$ | $\theta_{ref3}$ | $\theta_{ref4}$ | $\theta_{ref5}$ | $\theta_{ref6}$ | $\theta_{ref7}$ |
| 000 | - | - | - | - | + | + | + | + |
| 001 | + | - | - | - | - | + | + | + |
| 011 | + | + | - | - | - | - | + | + |
| 010 | + | + | + | - | - | - | - | + |
| 110 | + | + | + | + | - | - | - | - |
| 111 | - | + | + | + | + | - | - | - |
| 101 | - | - | + | + | + | + | - | - |
| 100 | - | - | - | + | + | + | + | - |

**Fig. 2.** Constellation of 8-PSK symbols and reference phases.

## 2. Single-bit sampling demodulation

Fig. 2 shows constellation of 8-PSK symbols represented by circles and reference phases by arrows ($\theta_{ref\,0-7}$). The phase of any input symbol can be determined by comparing input symbol phase with each of 8 reference phases. The phase comparison can be done by determining the sign of the phase difference between input symbol and each reference, or $\theta_{input}-\theta_{ref\,n}$. Fig. 2 shows the comparison result for each symbol in 8-PSK. This function can be realized in time domain by sampling input with multi-phase clock signals having reference phases. For example, if signs of $\theta_{input}-\theta_{ref\,n}$ are positive for $n=0, 1, 6, 7$ and negative for $n=2, 3, 4, 5$, then the input symbol is determined as 011. Since the result of phase comparison with $\theta_{ref\,4-7}$ is simply inversion of that with $\theta_{ref\,0-3}$ as shown in Fig. 2, only half of the reference phases, or multi-phase clocks, are needed in implementation. Fig. 3 shows timing diagrams for input symbol 011 with 4 multi-phase clock signals, $CK_{ref\,0-3}$. $CK_{ref\,0}$ and $CK_{ref\,1}$ produce sampled values of low, and $CK_{ref\,2}$ and $CK_{ref\,3}$ high. For each symbol of 8-PSK, sampled values are given in Fig. 3. Demodulation is complete when sampled values, LLHH, are decoded into the corresponding symbol, 011. Compared with conventional high-order PSK demodulation schemes based on multi-bit sampling analog-to-digital conversion




| Mode | Symbol | Sampled Value | | | |
|---|---|---|---|---|---|
| | | $CK_{ref0}$ | $CK_{ref1}$ | $CK_{ref2}$ | $CK_{ref3}$ |
| BPSK | 0 | H | X | X | X |
| | 1 | L | X | X | X |
| QPSK | 00 | H | X | H | X |
| | 01 | L | X | H | X |
| | 11 | L | X | L | X |
| | 10 | H | X | L | X |
| 8PSK | 000 | H | H | H | H |
| | 001 | L | H | H | H |
| | **011** | **L** | **L** | **H** | **H** |
| | 010 | L | L | L | H |
| | 110 | L | L | L | L |
| | 111 | H | L | L | L |
| | 101 | H | H | L | L |
| | 100 | H | H | H | L |

*H: High, L: Low, X: don't care*

**Fig. 3.** Timing diagrams of single-bit sampling (for input symbol 011).

and complex digital signal processing [16,17], our scheme consumes less power because it uses only single-bit samplers and simple phase comparison. In addition, since 8-PSK demodulator includes reference phases required for BPSK and QPSK, the demodulator operation mode can be easily changed when necessary using the decoding table given in Fig. 3. Since single-bit sampling is limited by the timing margin not by the amplitude, jitters on multi-phase clocks increase BER. In our proto-type chip, 16-PSK operation is implemented by doubling multiple phase clocks.

## 3. Implementation

Fig. 4a shows the block diagram of our prototype demodulator fabricated in TSMC 0.18-μm RF CMOS process. The receiver uses differential signaling to avoid 2nd-order distortions and achieve supply-noise immunity. The input signal is single-bit sampled by multiphase clocks generated from voltage-controlled oscillator (VCO). Sampled data are processed in the digital domain for symbol detection and phase extraction. The phase and frequency detector (PFD) unit offers up or down signal to the charge pump so that VCO phase is synchronized to the input signal for coherent operation. Compared to demodulators previously reported in [13–15], the demodulator in this work includes a CDR circuit, which rejects any ISI. Clock and data recovery (CDR) is employed to reject any inter-symbol interference (ISI) and provide clock synchronized to recovered data. The PSK decoder can be switched into BPSK, QPSK, 8-PSK or 16-PSK mode by an external control, and produces demodulated symbols as parallel data streams. CDR, PSK decoder and PFD unit are all implemented with auto placement and routing of standard logic cells. The core supply voltage for the prototype chip is lowered to 1.2 V using an internal supply regulator in order to reduce power consumption. For output and control signals, I/O and electrostatic discharge protection circuits are implemented using 3.3-V supply. Details of circuit implementation are given in Sections 3.1, 3.2 and 3.3. Fig. 4b shows the die photograph. The chip occupies 310 μm × 240 μm. Our target is 1.25-MSymbol/s symbol rate with 5-MHz carrier frequency.

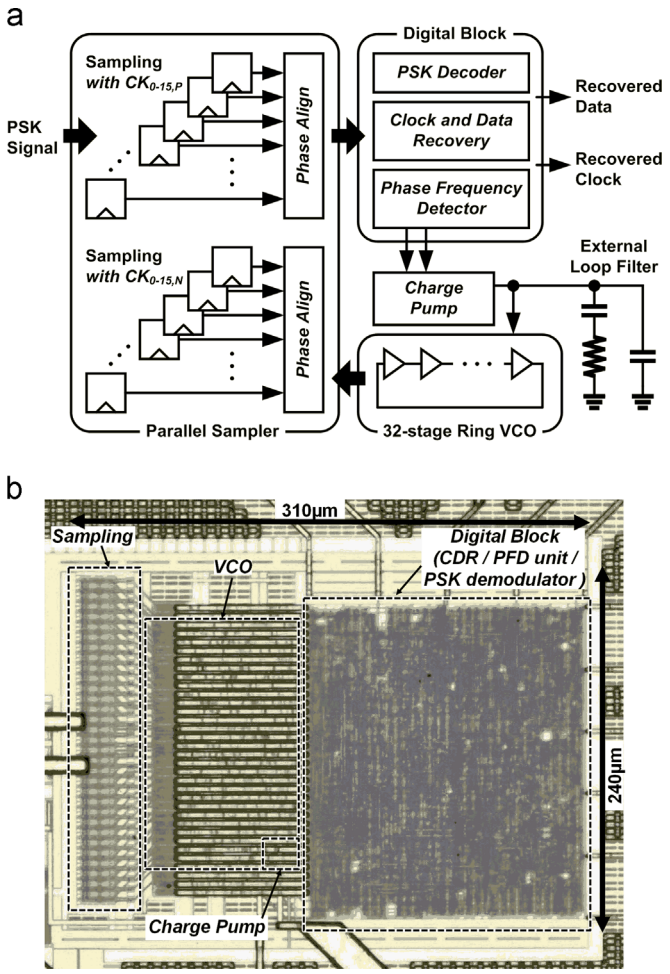



**Fig. 4.** (a) Block diagram of prototype demodulator. (b) Die photograph of prototype chip.

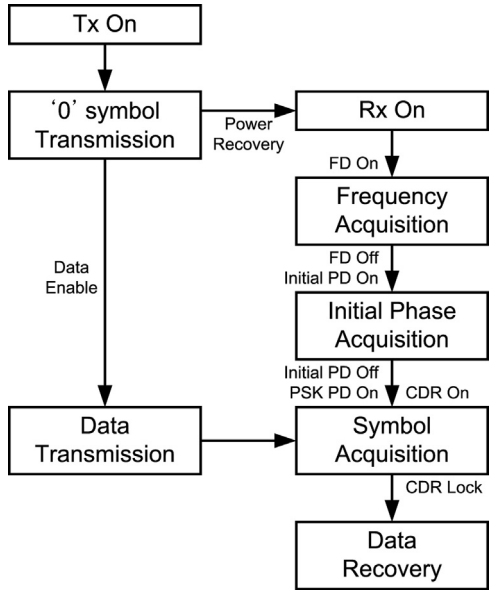



**Fig. 5.** Initializing process.

### 3.1. Analog circuits

Parallel sampler consists of single-bit samplers and phase aligners. Single-bit samplers are implemented using sense-amplifier-based flip-flops [18], which results in much reduced power consumption compared to samplers used in [13–15]. After multiphase sampling, sampled data are re-aligned for parallel processing by phase align blocks, which consists of D flip-flops. To improve timing resolution, the input signal is sampled at both rising and falling edges of multiphase clocks. Consequently, a multiphase-sampled set is produced at every rising and falling edges of 5-MHz clock, resulting in 10-MHz sampling frequency. In order to provide even-number multiphase clocks, VCO is implemented as 32-stage ring type. Ring-type oscillators are sensitive to process, voltage, and temperature (PVT) variations. However, they are designed with sufficient margin for control voltages so that the resulting oscillator produces the desired oscillation frequency even with PVT variations. In order to reduce mismatch between up and down currents of the charge pump, negative feedback is employed in the charge pump. Since the PFD unit in the receiver includes a bang-bang-type phase detector (PD) which usually requires large capacitance, the loop filter is externally attached to the prototype chip.

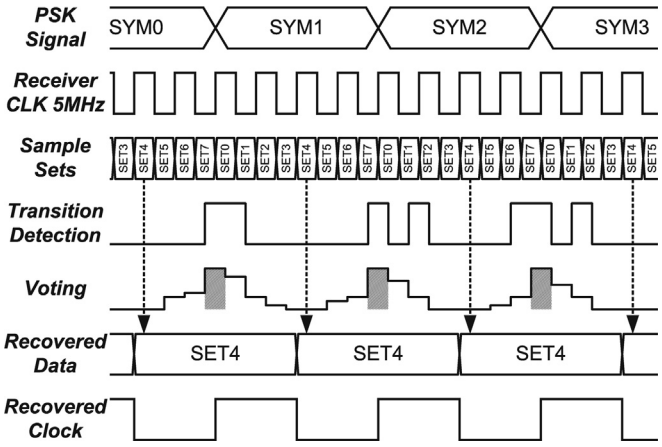



**Fig. 6.** Operation of CDR.

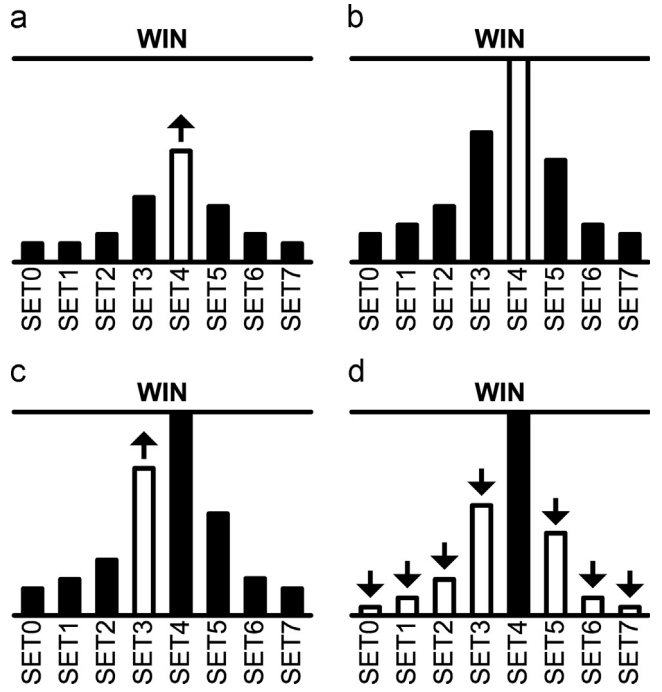



**Fig. 7.** Voting algorithm. (a) Before symbol acquisition. (b) Symbol acquisition is done. (c),(d) Continued voting race after symbol acquisition.

### 3.2. Frequency and phase acquisition

In order to achieve initial phase and frequency acquisition without employing a reference oscillator in the implanted unit, the prototype chip goes through the initializing process as shown in Fig. 5. Before data transmission, the transmitter sends the sinusoidal signal having the phase of symbol '0' that wakes up the receiver. Frequency detection in the PFD unit is realized by counting the number of transition edges of the input signal during one period of the receiver clock. Since the sampling block provides multiphase-sampled data sets, edge counting is implemented with XOR gates and adders. The receiver aligns its clock phase to the input sinusoidal signal having the phase of symbol '0' for initial phase acquisition, since symbol decision is made by the phase difference from the initial phase. Then, the receiver turns on the PD in the PFD unit for the PSK mode selected by the external control in order to maintain phase locked status for any symbol phases. 1/M-rate PDs commonly used in baseband applications are applicable to phase-locking of M-PSK signal, and BPSK demodulators using 1/2-rate PD [13] and QPSK demodulators using 1/4-rate PD [14,15] have been reported. The designed PFD module selects 1/2-, 1/4-, 1/8- or 1/16-rate phase detector corresponding to the

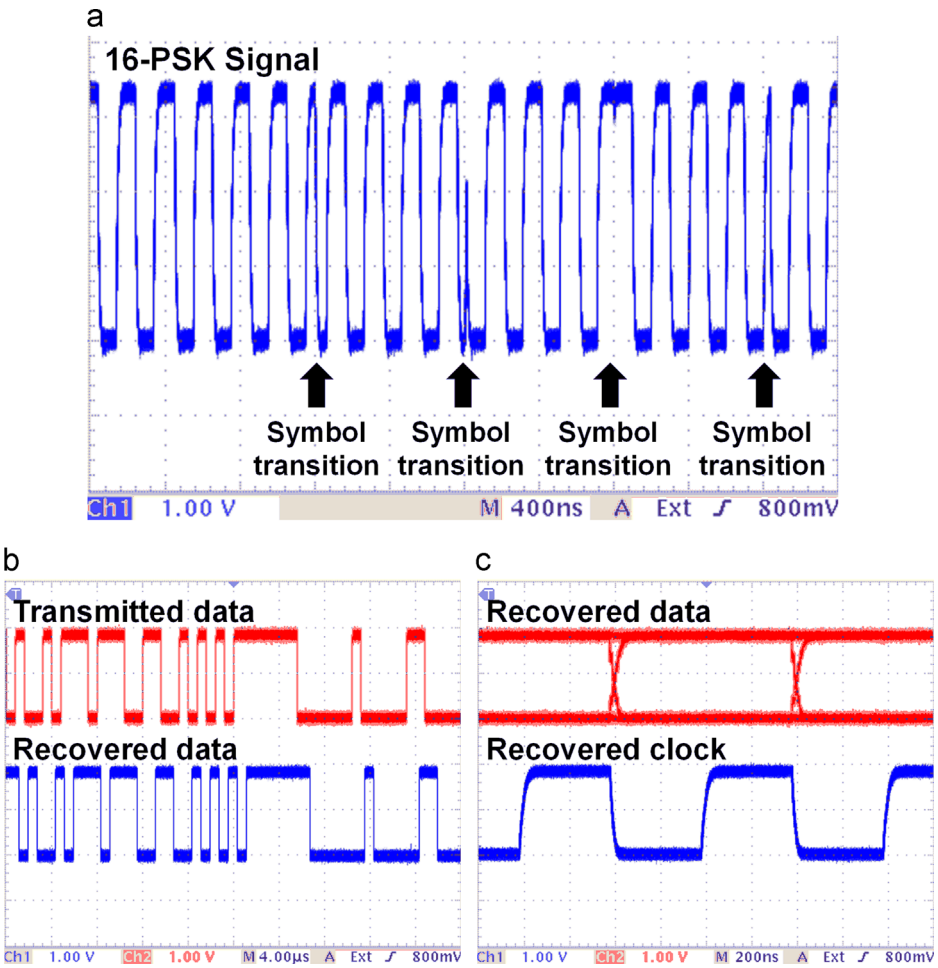



**Fig. 8.** (a) 16-PSK signal used as the input of the prototype chip. (b) A pair of 4 transmitted and recovered data streams for 16-PSK in inductive link. (c) Recovered data eye-diagram and recovered clock. (I/O supply: 3.3 V).

**Table 1**
Performance comparison with previously reported demodulators.

| | [7] | [8] | [9] | [10] | [11] | [12] | **This work**[a] |
|---|---|---|---|---|---|---|---|
| **Year** | 2006 | 2005 | 2008 | 2008 | 2010 | 2011 | **2011** |
| **Process [µm]** | 0.6 | 0.18 | 0.18 | 0.5 | 0.18 | 0.5 | **0.18** |
| **Modulation** | FSK | BPSK | BPSK | BPSK | OQPSK | PHM | **BPSK/QPSK/8-PSK/16-PSK** |
| **Maximum data rate [Mb/s]** | 2.083 | 1.12 | 0.8 | 0.02 | 4.16 | 10.2 | **5 (16-PSK)** |
| **Carrier frequency [MHz]** | 5.21 (4.17 /6.25) | 10 | 4 | 13.56 | 13.56 | – | **5** |
| **Power consumption [mW]** | 0.25 | 0.61 | 0.059 | 3 | 0.68 | 3 | **0.168**[a] |
| **Supply voltage [V]** | 5 | 1.8 | 1.8 | 3.3 | 1.8 | 3.3 | **1.2** |
| **Area [mm$^2$]** | 0.03 | 0.19 | 0.0043 | 0.099 | 0.2379 | 0.5076 | **0.0924**[a] |
| **Maximum data rate per carrier frequency [(b/s)/Hz]** | 0.4 | 0.112 | 0.2 | 0.0015 | 0.307 | – | **1** |
| **Energy per bit [nJ/bit]** | 0.1 | 0.545 | 0.074 | 150 | 0.163 | 0.294 | **0.034**[a] |

[a] Including CDR.

external control. The transmitter begins data transmission and the receiver finds symbol transition edges using CDR. After CDR recognizes that symbol acquisition is complete, the receiver produces recovered data and clock.

### 3.3. CDR

The CDR function is realized with the blind-oversampling structure [19]. Since multiphase-sampled data sets are produced with 10-MHz sampling frequency, 1.25-MSymbol/s input data are 8× oversampled. Fig. 6 shows the operation of CDR. The input signal produces one multiphase-sampled set at every rising or falling edge of the receiver clock, resulting in 8 sets (SET0-7) in one symbol period. Transitions are detected by recognizing difference between two adjacent sample sets. Since the input signal contains noise and ISI, transitions usually appear around, not only at, symbol transitions. Consequently, the transition point should be confirmed by a vote. Fig. 6 shows a case in which the transition point is found between SET7 and SET0 by voting. Although the error probability is smallest at the farthest point from the transition, even-number oversampling does not sample that point as can be seen in the figure where the farthest point from the transition is located between SET3 and SET4. In our CDR, the latter one, or SET4 in the figure, is selected as the data-decision point.

In our CDR, the transition point is continuously updated by voting. Fig. 7a shows the voting algorithm, in which the stacked value of the transition-detected point (SET4) increases by one. When the stacked value at any point reaches WIN (63 in this design) as shown in Fig. 7b, CDR realizes that symbol acquisition is done and selects the data decision point. Then, it starts to produce recovered data and clock and the voting continues. In the real design, this voting function can be done only in the training period or periodically as defined in the system level in order to minimize power consumption. If a transition is detected at another point (SET3) as shown in Fig. 7c, the stacked value at that point increases by one. If transition is detected at WIN position (SET4) as shown in Fig. 7d, other stacked values decrease by one.

## 4. Measurement

To verify the operation as a demodulator, we measured BER in the back-to-back connection between the PSK modulator and our prototype chip. Our demodulator successfully demodulates 1.25-MSymbol/s BPSK, QPSK, 8-PSK, and 16-PSK signals at 5-MHz carrier frequency with the maximum total data rate of 5 Mb/s for 16-PSK without any error. The prototype chip consumes 140 μA from 1.2-V regulated supply. For 16-PSK signal shown in Fig. 8a, a pair of 4 transmitted and recovered parallel data streams is shown in Fig. 8b, which shows input data are successfully demodulated. The recovered data eye-diagram and the recovered clock signal are shown in Fig. 8c. The rising edge of the recovered clock is aligned to the center of recovered data. The performance of our demodulator is compared with those of previously reported demodulators for inductive links applications in Table 1. As can be seen in the table, there have been various attempts to realize various types of demodulators that are spectrally efficient and low-power for biomedical implant applications. Compared to previously reported demodulators, our demodulator achieves higher data rate per carrier frequency (b/s)/Hz while having much lower energy per bit, even if it contains CDR block, which should be of great advantage for many biomedical implant application.

## 5. Conclusion

In this paper, we demonstrated a new type of PSK demodulator that can be used for biomedical implants. Our PSK demodulation scheme uses single-bit sampling, resulting in very low power consumption. The prototype chip fabricated in 0.18-μm CMOS technology successfully demodulated 5-Mb/s 16-PSK data at 5-MHz carrier frequency. It is expected that the spectral efficiency of biomedical implants is improved by employing the proposed high-order PSK demodulator with low power consumption. That contributes to both the efficient power telemetry and the high data rate transmission.

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